Appl. No. 10/751,283
Amdt. dated November 1, 2005
Reply to Office Action of August 1, 2005

PATENT

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1   Claim 1. (currently amended) A programmable logic device, comprising a
2   plurality of logic elements and a routing structure, wherein the routing structure comprises a
3   plurality of routing lines, and wherein each routing line comprises:
4   a plurality of first OR gates, each first OR gate having at least a first input
5   connected to a respective one of said logic elements in a first group of said logic elements, and
6   each first OR gate except a final first OR gate in said line having an output connected to a second
7   input of a respective succeeding one of said first OR gates, such that a signal from one of said
8   logic elements in the first group of logic elements appears on an output of the final first OR gate
9   in said line; and
10   <u>a return line, comprising a plurality of drivers connected in series, each of said</u>
11   <u>drivers having a</u> connection[s] to a <u>respective one of a</u> plurality of said logic elements in a
12   second group of logic elements, such that the signal appearing on said output of the final first OR
13   gate in said line may be passed to said plurality of logic elements in the second group of logic
14   elements.

1   Claim 2. (original) A programmable logic device as claimed in claim 1, wherein
2   the first group of logic elements and the second group of logic elements are mutually exclusive.

1   Claim 3. (original) A programmable logic device as claimed in claim 1, wherein
2   the first group of logic elements and the second group of logic elements contain at least one logic
3   element in common.

1   Claim 4. (original) A programmable logic device as claimed in claim 1, wherein
2   the logic elements in said programmable logic device are arranged in an array, the array
3   comprising rows and columns of logic elements.

Appl. No. 10/751,283
Amdt. dated November 1, 2005
Reply to Office Action of August 1, 2005

PATENT

1   Claim 5. (original) A programmable logic device as claimed in claim 4, wherein

2   the first group of logic elements are located within a first row of said array.

1   Claim 6. (original) A programmable logic device as claimed in claim 5, wherein

2   the second group of logic elements are located within said first row of said array.

1   Claim 7. (original) A programmable logic device as claimed in claim 5, wherein

2   the second group of logic elements are located within a second row of said array different from

3   said first row.

1   Claim 8. (original) A programmable logic device as claimed in claim 5, wherein

2   the first group of logic elements are spaced apart at regular intervals within said first row of said

3   array.

1   Claim 9. (original) A programmable logic device as claimed in claim 7, wherein

2   the second group of logic elements are spaced apart at regular intervals within said second row of

3   said array.

1   Claim 10. (original) A programmable logic device as claimed in claim 4, wherein

2   the first group of logic elements are located within a first column of said array.

1   Claim 11. (original) A programmable logic device as claimed in claim 10,

2   wherein the second group of logic elements are located within said first column of said array.

1   Claim 12. (original) A programmable logic device as claimed in claim 10,

2   wherein the second group of logic elements are located within a second column of said array

3   different from said first column.

1   Claim 13. (original) A programmable logic device as claimed in claim 10,

2   wherein the first group of logic elements are spaced apart at regular intervals within said first

3   column of said array.

Appl. No. 10/751,283
Amdt. dated November 1, 2005
Reply to Office Action of August 1, 2005

PATENT

1   Claim 14. (original) A programmable logic device as claimed in claim 12,

2   wherein the second group of logic elements are spaced apart at regular intervals within said

3   second column of said array.

1   Claim 15. (currently amended) A programmable logic device, comprising:

2   a plurality of logic elements arranged in an array, the array comprising rows and

3   columns of logic elements, the rows of said array being located at respective vertical positions in

4   said array, and the columns of said array being located at respective horizontal positions in said

5   array; and

6   a routing structure, wherein the routing structure comprises a first plurality of

7   routing lines, running parallel to said rows of logic elements at a first vertical position in said

8   array; a second plurality of routing lines, running parallel to said rows of logic elements at a

9   second vertical position in said array; a third plurality of routing lines, running parallel to said

10 columns of logic elements at a first horizontal position in said array; and a fourth plurality of

11 routing lines, running parallel to said columns of logic elements at a second horizontal position

12 in said array,

13   wherein each routing line comprises:

14   a plurality of first OR gates, each first OR gate having at least a first input

15 connected to a respective one of said logic elements in a respective first group of said logic

16 elements, and each first OR gate except a final first OR gate in said line having an output

17 connected to a second input of a respective succeeding one of said first OR gates, such that a

18 signal from one of said logic elements in the first group of logic elements appears on an output of

19 the final first OR gate in said line; and

20   a return line, comprising a plurality of drivers connected in series, each of said

21 drivers having a connection[s] to a plurality of said logic elements in a respective second group

22 of logic elements, such that the signal appearing on said output of the final first OR gate in said

23 line may be passed to said plurality of logic elements in the second group of logic elements.

Appl. No. 10/751,283
Amdt. dated November 1, 2005
Reply to Office Action of August 1, 2005

PATENT

1   Claim 16. (original) A programmable logic device as claimed in claim 15,

2   wherein routing lines of said first plurality of routing lines and of said second plurality of routing

3   lines are connected to respective logic elements spaced apart along said rows of logic elements;

4   and

5   routing lines of said third plurality of routing lines and of said fourth plurality of

6   routing lines are connected to respective logic elements spaced apart along said columns of logic

7   elements.

1   Claim 17. (currently amended) A programmable logic device, comprising a

2   plurality of logic elements and a routing structure, wherein the routing structure comprises a

3   plurality of distributed OR gates, each distributed OR gate comprising logic circuitry having a

4   plurality of inputs from a first plurality of logic elements distributed amongst said logic elements

5   and forming a logic OR function from said inputs, and an output of each distributed OR gate

6   being connected to a second plurality of logic elements distributed amongst said logic elements,

7   wherein the routing structure is distinct from a programmable interconnect structure of the

8   programmable logic device.

1   Claim 18. (currently amended) In a programmable logic device, comprising a

2   plurality of logic elements and a routing structure, wherein the routing structure comprises a

3   plurality of distributed OR gates, each distributed OR gate comprising logic circuitry having a

4   plurality of inputs from a first plurality of logic elements distributed amongst said logic elements

5   and forming a logic OR function from said inputs, and an output of each distributed OR gate

6   being connected to a second plurality of logic elements distributed amongst said logic elements,

7   a method of forming a bus structure, the method comprising:

8   allocating functionality to said first plurality of logic elements, and to said second

9   plurality of logic elements in a first distributed OR gate; and

10   controlling said first plurality of logic elements such that they each output a

11   logical zero except when involved in a data transaction,

Appl. No. 10/751,283
Amdt. dated November 1, 2005
Reply to Office Action of August 1, 2005

PATENT

12   such that outputs from said first plurality of logic elements are multiplexed

13 together, and made available to said second plurality of logic elements <u>via a return line coupled</u>

14 <u>to an end OR gate of the plurality of distributed OR gates</u>.

1   Claim 19. (original) A method of forming a bus structure, as claimed in claim 18,

2 further comprising:

3   allocating additional functionality to said first plurality of logic elements, and to

4 said second plurality of logic elements, such that said second plurality of logic elements are

5 connected to the inputs of a second distributed OR gate and the output of the second distributed

6 OR gate is connected to the first plurality of logic elements; and

7   controlling said second plurality of logic elements such that they each output a

8 logical zero except when involved in a data transaction,

9   such that outputs from said second plurality of logic elements are multiplexed

10 together, and made available to said first plurality of logic elements.

1   Claim 20. (original) A method of forming a bus structure, as claimed in claim 19,

2 comprising allocating functionality to said first plurality of logic elements such that they form

3 parts of respective bus master devices, and allocating functionality to said second plurality of

4 logic elements such that they form parts of respective slave devices in said bus structure.